connecting the middle node to a voltage source corresponding to the third voltage level in response to a control signal indicating that the integrated circuit is placed in the first power state.

3. The method of claim 2 further comprising:

disconnecting the middle node from the voltage source in response to the control signal indicating that the integrated circuit is placed in the second power state.

4. The method of claim 3 wherein the control signal is set to a first value if the integrated circuit is in the first power state and set to a second value if the integrated circuit is in the second power state.

5. The method of claim 3 wherein connecting the middle node to the voltage source comprises:

turning on a switching device to connect the middle node to the voltage source.

6. The method of claim 5 wherein disconnecting the middle node from the voltage source comprises:

turning off the switching device to disconnect the middle node from the voltage source.

7. The method of claim 6 wherein the switching device comprises a transistor.

8. The method of claim 1 wherein the first and second capacitors are selected from the group consisting of oxide-nitride-oxide (ONO) capacitors and metal-oxide-semiconductor (MOS) capacitors.

9. The method of claim 1 wherein the capacitance of the first capacitor is approximately equal to the capacitance of the second capacitor.

10. (Currently Amended) A method of controlling the voltage levels across capacitors coupled between a first node and a second node of an integrated circuit so that the voltage levels across these capacitors will not exceed the breakdown voltage limitation of these capacitors, the voltage level between the first and second nodes varying from a second voltage level to a first voltage level when the integrated circuit transitions from a second power state to a first power state, the method comprising:

connecting in series a first capacitor and second capacitor between the first and second nodes of the integrated circuit forming a middle node between the first and second capacitors; and

setting the voltage level of the middle node to a third voltage level when the integrated circuit is placed in the first power state such that the voltage level between the first and middle nodes does not exceed the breakdown voltage of the first capacitor and the voltage level between the middle and second nodes does not exceed the breakdown voltage of the second capacitor, the third voltage level at the middle node corresponds to the voltage level at the first node when the integrated circuit is placed in the first power state.

11. The method of claim 10 wherein the middle node is connected to the first node via a switching device when the integrated circuit is placed in the first power state.

12. The method of claim 11 wherein the middle node is disconnected from the first node via the switching device when the integrated circuit is placed in the second power state.

13. The method of claim 12 wherein the switching device is turned on in response to a control signal indicating that the integrated circuit is in the first power state and turned off in response to the control signal indicating that the integrated circuit is in the second power state.

14. The method of claim 13 wherein the switching device comprises a transistor.

15. (Currently Amended) In a charge pump having a plurality of pump stages connected in series, at least one of the pump stages including at least one node to be coupled to a

corresponding clock signal via a capacitive device, the at least one node having a first voltage when the charge pump is in a first power state and a second voltage when the charge pump is in a second power state, a method of balancing [the] a voltage requirement at the at least one node with [the] stress limitation and die area of the capacitive device[, the method] comprising:

using a single capacitor of a first type as the capacitive device between the at least one node and the corresponding clock signal if the first voltage and the second voltage do not exceed the stress limitation of the single capacitor of the first type;

if the second voltage exceeds the stress limitation of the single capacitor of the first type, using a single capacitor of a second type as the capacitive device between the at least one node and the corresponding clock signal if the first voltage and the second voltage do not exceed the stress limitation of the single capacitor of the second type, the single capacitor of the second type having greater stress limitation and greater die area than the single capacitor of the first type; and

if the second voltage exceeds the stress limitation of the single capacitor of the second type, using two capacitors of the first type connected in series as the capacitive device between the at least one node and the corresponding clock signal if the first voltage and the second voltage do not exceed the combined stress limitation of the two capacitors of the first type; and

if the first voltage exceeds the combined stress limitation of the two capacitors of the first type, setting the middle node between the two capacitors of the first type to a third voltage level when the charge pump is in the first power state such that the voltage across each of the two capacitors does not exceed the stress limitation of the respective capacitor, the third voltage level at the middle node corresponds to the voltage level at the first node when the charge pump is placed in the first power state.

16. The method of claim 15 wherein setting the middle node between the two capacitors to the third voltage level comprises:

connecting the middle node to a voltage source corresponding to the third voltage level via a

switching device in response to a control signal indicating that the charge pump is placed in the first power state.

17. The method of claim 15 further comprising:

disconnecting the middle node from the voltage source corresponding to the third voltage level via the switching device in response to the control signal indicating that the charge pump is placed in the second power state.

18. A charge pump circuit including a plurality of pump stages being connected in series each having an input node and an output node, at least one of the pump stages comprising:

a switching transistor having a gate, a first terminal, and a second terminal, the first terminal being coupled to the input node of the respective pump stage and the second terminal being coupled to the output node of the respective pump stage;

a first capacitor having a first end and a second end, the first end of the first capacitor being coupled to the gate of the switching transistor;

a second capacitor having a first end and a second end, the first end of the second capacitor being coupled to the second end of the first capacitor forming a first intermediate node, the second end of the second capacitor being coupled to a first clock signal;

a third capacitor having a first end and a second end, the first end of the third capacitor being coupled to the output node of the respective pump stage; and

a fourth capacitor having a first end and a second end, the first end of the fourth capacitor being coupled to the first end of the third capacitor forming a second intermediate node, the second end of the fourth capacitor being coupled to a second clock signal

wherein the first and second intermediate nodes are set to a predetermined voltage level when the

charge pump circuit is placed in a low power state.

19. The charge pump circuit of claim 18 wherein the first and second intermediate nodes are set to the predetermined voltage level via a switching device in response to a control signal indicating that the charge pump circuit is placed in the low power state.

20. The charge pump circuit of claim 19 wherein the switching device comprises a first control transistor and a second control transistor, the first and second control transistors being turned on in response to the control signal indicating that the charge pump circuit is placed in the low power state to connect the first intermediate and second intermediate nodes, respectively, to a voltage source corresponding to the predetermined voltage level.

21. The charge pump circuit of claim 20 wherein the voltage source is set to a first voltage level to turn on the first and second control transistors when the charge pump circuit is placed in the low power state and to a second voltage level to turn off the first and second control transistors when the charge pump circuit is placed in a high power state.

22. A charge pump stage in a charge pump circuit, the charge pump stage comprising:

a first switching transistor having a gate, a first terminal and a second terminal, the first terminal being coupled to an input node of the charge pump stage, the second terminal being coupled to an output node of the charge pump stage;

at least two capacitors connected in series between the gate of the first switching transistor and a first clock signal forming a first intermediate node between the two capacitors;

at least two capacitors connected in series between the output node and a second clock signal forming a second intermediate node between the two capacitors;

a control device to connect the first and second intermediate nodes to a first voltage source when the charge pump circuit is in a first power state and to disconnect the first and second

intermediate nodes from the first voltage source when the charge pump circuit is in a second power state;

a first diode having an input terminal and an output terminal, the input terminal being coupled to the first terminal of the first switching transistor and the output terminal being coupled to the gate of the first switching transistor; and

a second diode having an input terminal and an output terminal, the input terminal being coupled to the gate of the first transistor, the output terminal being coupled to the first terminal of the first switching transistor.

23. The charge pump stage of claim 22 wherein the control device comprises a first control transistor and a second control transistor, the first and second control transistors being turned on in response to a control signal indicating that the charge pump circuit is in the first power state, the first and second control transistors being turned off in response to the control signal indicating that the charge pump circuit is in the second power state.

24. The charge pump stage of claim 23 wherein the first voltage source is used as the control signal, the first voltage source being set to a first value when the charge pump circuit is in the first power state and being set to a second value when the charge pump circuit is in the second power state.

25. (New) A method comprising:

connecting first and second capacitors between first and second nodes of an integrated circuit to form a middle node between the first and second capacitor; and
setting a voltage at the middle node to a first voltage level when the integrated circuit is in a first power state so that a voltage level between the first and middle nodes does not exceed a breakdown voltage of the first capacitor, and a voltage level between the middle and second nodes does not exceed a breakdown voltage of the second capacitor, the first and second power states corresponding to low and high power states, respectively.

26. (New) The method of claim 25 wherein setting the voltage at the middle node comprises:

connecting the middle node to a voltage source corresponding to the first voltage level in response to a control signal indicating that the integrated circuit is placed in the first power state.

27. (New) The method of claim 26 further comprising:

disconnecting the middle node from the voltage source in response to the control signal indicating that the integrated circuit is placed in the second power state.

28. (New) The method of claim 27 wherein the control signal is set to a first value if the integrated circuit is in the first power state and set to a second value if the integrated circuit is in the second power state.

29. (New) The method of claim 27 wherein connecting the middle node to the voltage source comprises:

turning on a switching device to connect the middle node to the voltage source.

30. (New) The method of claim 29 wherein disconnecting the middle node from the voltage source comprises:

turning off the switching device to disconnect the middle node from the voltage source.

31. (New) The method of claim 30 wherein the switching device comprises a transistor.

32. (New) The method of claim 25 wherein the first and second capacitors are selected from the group consisting of oxide-nitride-oxide (ONO) capacitors and metal-oxide-semiconductor (MOS) capacitors.

33. (New) The method of claim 25 wherein the capacitance of the first capacitor is approximately equal to the capacitance of the second capacitor.

34. (New) A system comprising:

a phase generator to provide first and second clock signals;

an integrated circuit; and

a charge pump circuit including a pump stage having an input node and an output node, the output node providing power to the integrated circuit, at least one of the pump stages comprising:

a switching transistor having a gate, a first terminal and a second terminal, the first terminal being coupled to the input node of the pump stage and the second terminal being coupled to the output node of the pump stage,

a first capacitor having a first end and a second end, the first end of the first capacitor being coupled to the gate of the switching transistor,

a second capacitor having a first end and a second end, the first end of the second capacitor being coupled to the second end of the first capacitor forming a first intermediate node set to a predetermined voltage level when the change pump circuit is placed in a low power state, the second end of the second capacitor being coupled to the phase generator to receive the first clock signal,

a third capacitor having a first end and a second end, the first end of the third capacitor being coupled to the output node of the pump stage, and

a fourth capacitor having a first end and a second end, the first end of the fourth capacitor being coupled to the first end of the third capacitor forming a second intermediate node set to the predetermined voltage level when the charge pump circuit is placed in the low power state, the second end of the fourth capacitor being coupled to the phase generator to receive the second

clock signal.

35. (New) The system of claim 34, wherein the charge pump circuit further comprises a switching device to set the first and second intermediate nodes to the predetermined voltage level via a switching device in response to a control signal indicating that the charge pump circuit is placed in the low power state.

36. (New) The system of claim 35, wherein the switching device of the charge pump circuit comprises a first control transistor and a second control transistor, the first and second control transistors being turned on in response to the control signal indicating that the charge pump circuit is placed in the low power state to connect the first intermediate and second intermediate nodes, respectively, to a voltage source supplying the predetermined voltage level.

37. (New) The system of claim 36, wherein the voltage source is set to a first voltage level to turn on the first and second control transistors when the charge pump circuit is placed in the low power state and to a second voltage level to turn off the first and second control transistors when the charge pump circuit is placed in a high power state.

CONCLUSION

In accordance with 37 CFR §1.173(b), Applicant respectfully submits herewith the proposed amendments for incorporation into the above-identified reissue application. Reconsideration of pending claims 1-37 is respectfully requested.

Respectfully submitted,

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